REMARKS

Claims 1-4 are pending in this application, all of which have been amended. No new claims have been added.

The Examiner has objected to claims 1-4 for an informality which has been corrected in the aforementioned amendments.

Before turning to the cited references, a brief review of the claimed invention is in order.

According to a dielectric filter recited in claim 1, as amended, of the instant application, a pair of input and output electrodes 6, 6 are opposed to each other on one plane providing the outer peripheral surface of a dielectric block 1, and a dielectric block exposing portion 13 is formed all over the region of said one plane between the input and output electrodes 6, 6 and having no conductor layer thereon.

Therefore, a second capacitance coupling between the pair of input and output electrodes 6, 6 is provided, and causes an additional attenuation pole d2 to appear anew. The frequencies of the attenuation pole d2 can be adjusted by varying the distance T between the input and output electrodes. This makes it possible to design filters adapted for use in a multiple of various frequency bands.

Claims 1-4 stand rejected under 35 USC §103(a) as unpatentable over Applicants' Admitted Prior Art (hereinafter "**APA**") or U.S. Patent 5,652,555 to Tada et al. (hereinafter

"**Tada et al.**") in view of U.S. Patent 6,784,767 to Hiroshima et al. (hereinafter "**Hiroshima et al.**").

Applicants respectfully traverse this rejection.

Tada et al. discloses a compact dielectric band elimination filter using a resonator apparatus having a dielectric block with a plurality of throughholes each containing an inner conductor and serving as a resonator. Capacitor electrodes are formed on a main surface of the block such that series-connected resonant capacitors are provided with the inner conductors inside the throughholes. The resonator apparatus is mounted on a substrate of a layered structure having an inductor thereon. Each trap frequency of the filter associated with one of the resonators can be adjusted by making adjustments on the associated resonator without affecting the characteristics of the adjacent resonators, by forming a larger-diameter part and a smaller-diameter part separated by a step inside each throughhole or by using a dielectric block having a wider part and a narrower part through which throughholes with a uniform inner diameter are formed, such that the even-mode input impedance and odd-mode input impedance of each resonator will be equal to zero at the trap frequency associated therewith.

Hiroshima et al. discloses a dielectric filter including a dielectric block having inner-conductor-formed holes extending from a first face of the dielectric block to a second face opposed to the first face. Inner conductors are formed inside the inner-conductor-formed holes such that both ends of the inner-conductor-formed holes are open-circuited. On the exterior

surface of the dielectric block, balanced input/output terminals are capacitively coupled to the open ends of the inner-conductor-formed holes. A metal cover is provided so as to cover one of the first or second face of the dielectric block. The metal cover functions as a short-circuit conductor in a spurious mode such as a TE mode other than a TEM mode, and hence the influence of the spurious mode is avoided.

The Examiner has admitted that neither **APA** nor **Tada et al.** teaches, mentions or suggests a groove on the open end face of the dielectric block and in conduction with the outer conductor, but has cited **Hiroshima et al.** for teaching this feature (Fig. 8).

Even admitting this feature, Applicants respectfully submit that none of the cited references teaches, mentions or suggests that no conductor layer appears on the dielectric block exposing portion 13 being formed all over the outer peripheral surface of the dielectric blank between the input and output electrodes, as shown in Fig. 1 of the instant application. Accordingly, claim 1 has been amended to clarify this distinction. **Tada et al.**, in fact, also fails to disclose the "outer conductor in the form of a conductor layer and covering an outer peripheral surface of the block in parallel with the extending direction of the through bores and one end face of the block," as recited in claim 1 of the instant application.

Furthermore, in contrast to the present invention, according to a dielectric filter disclosed in either **APA**, **Hiroshima et al.**, **Tada et al.**, or **Ishikawa et al.**, at least one conductor layer is formed on the outer peripheral surface of a dielectric block between input and output electrodes.

Thus, the 35 USC §103(a) rejection should be withdrawn.

Claims 1-4 stand rejected under 35 USC §103(a) as unpatentable over **APA** or **Tada et al.** in view of U.S. Patent 4,733,208 to Ishikawa et al. (hereinafter "**Ishikawa et al.**").

Applicants respectfully traverse this rejection.

The Examiner has urged that **Ishikawa et al.** shows, in Fig. 17, a groove 20a arranged between electrode 22a and the opposing electrode (unnumbered), but, like the other cited references discussed above, fails to teach, mention or suggest that no conductor layer appears on the dielectric block exposing portion 13 between the electrodes.

Thus, the 35 US §103(a) rejection should be withdrawn.

In view of the aforementioned amendments and accompanying remarks, claims 1-4, as amended, are in condition for allowance, which action, at an early date, is requested.

If, for any reason, it is felt that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney at the telephone number indicated below to arrange for an interview to expedite the disposition of this case.

In the event that this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Substitute Abstract of the Disclosure
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